A 32 TAP DIGITALLY CONTROLLED PROGRAMMABLE TRANSVERSAL FILTER USING LSI GaAs ICs

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ABSTRACT

A Digitally Controlled Programmable Transversal Filter (DCPTF) is described that employs a $LiNbO_3$ SAW delay line and two LSI GaAs ICs to digitally control magnitude and sign of the 32 tap weights. The DCPTF constitutes a significant reduction in size over the previously reported PTF with little sacrifice in performance. The DCPTF is completely programmable and is constrained only by the bandwidth (100 MHz centered at 300 MHz) and the number of taps.

INTRODUCTION

The Digitally Controlled Programmable Transversal Filter is an extremely versatile wideband signal processor. This single device operates as a bandpass, band-reject, adaptive, or matched filter [1].

Previously, a Hybrid Programmable Transversal Filter was described that employed a $LiNbO_3$ SAW delay line and two dual-gate FET arrays [2, 3]. However, this approach requires 64 external D/A converters for programming, making it impractical in a compact Adaptive Interference Suppression system.

The DCPTF described herein is the next generation to this approach. Two 32 tap filters were built which operate over a 100 MHz bandwidth (33%) centered at 300 MHz. The DCPTF replaces the dual-gate FET arrays and external D/A converters with LSI GaAs ICs that enable direct interfacing to TTL signals.

SAW-PTF CONCEPT

The Digitally Controlled Programmable Transversal Filter consists of a tapped SAW delay line whose output electrodes are connected to two identical arrays of programmable tap weight control amplifiers as shown in Figure 1. The RF signal is applied to an input transducer, which generates a surface acoustic wave that propagates down the $LiNbO_3$ substrate to an array of output electrodes. Each output electrode detects the electrical signal associated with the acoustic wave. Because of the 4.2 nsec delay between output electrodes, each electric signal is a delayed copy of the original input. The signal then flows into the RF tap weighting amplifier

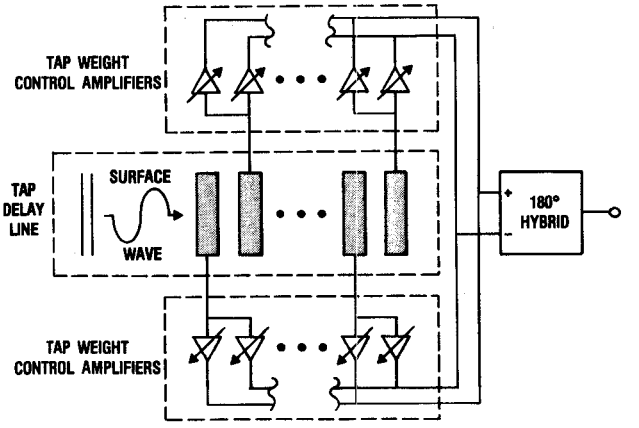

Figure 1. SAW-PTF Block Diagram.

input. The amplifier outputs of each phase are connected to their respective summing bus. Negative tap weights are generated with an external 180^0 hybrid.

LSI GaAs IC

Each RF tap weight control amplifier consists of a segmented dual-gate FET [4] where the gain of each FET is binarily scaled, as shown in Figure 2. For example, the gain of the first FET is $2^0 = 1$ while the gain of the seventh FET is $2^6 = 64$. Gate-2 voltages are used for gain programming, but each FET is programmed either to its maximum gain (on state) or

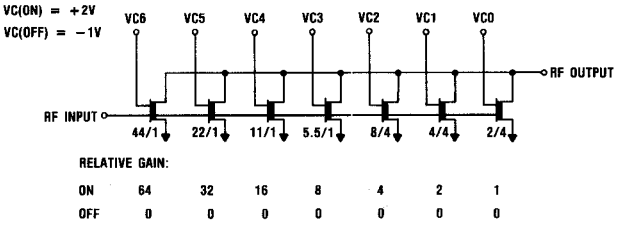

Figure 2. Segmented Dual Gate FET.

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to zero gain (off state). Since all FETs are in parallel, the overall amplifier gain is the sum of the gains of the FETs that are programmed to the on state. So each gate-2 line controls one bit (binary representation) of the desired tap weight. The amplifier is capable of being programmed discretely to any gain from 0 to 127. The seven FETs are programmed by a seven bit digital bus and form a digitally controlled variable gain amplifier (DCVGA). When connected to the external (off chip) 180° hybrid, this arrangement is programmed discretely to any gain from −1 to + 1 with 7 bit resolution.

The digitally controlled variable gain amplifier eliminates the analog control voltages and hence the external D/As. However, the number of control lines has been increased by a factor of 7 (324 for a 16 tap LSI GaAs IC array). Therefore, some kind of on-chip data multiplexing and storage is required. To solve this problem, each pair of dual-gate FETs (+ and −) share a static storage cell (Figure 3). Each storage cell has a "Load" line and a data line. There are 7 data lines, one for each bit, and one load line for each tap. The arrangement of a positive weight amplifier, a negative amplifier, and seven memory cells makes up a unit cell.

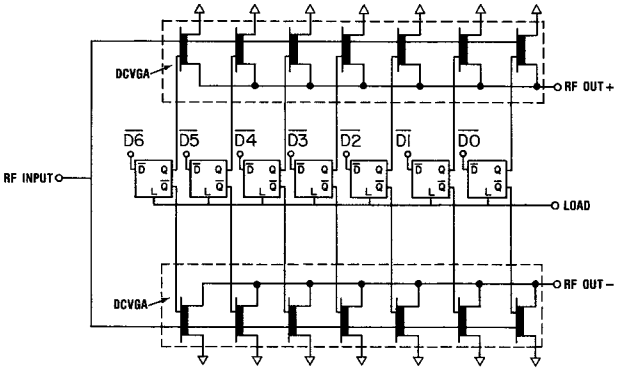

Figure 3. Variable Gain Amplifier Unit Cell.

The digital inputs to the unit cell are at nonstandard voltage levels so TTL interface buffers have been designed. These buffers were fabricated separately from the unit cell, but on the same slice, and can be bonded to the digital inputs to provide TTL interfacing.

The 16 tap DCVGA block diagram is shown in Figure 4. The array consists of 16 unit cells connected by a common 7 bit data bus. Tap weights are presented on the data bus and selectively loaded into the memory cells of a unit cell by strobing the "Load" line high. This sets the + and − tap weighting for that respective unit cell. With the address decoder the input requirements have been reduced to 7 data lines, 4 address lines and 1 chip select.

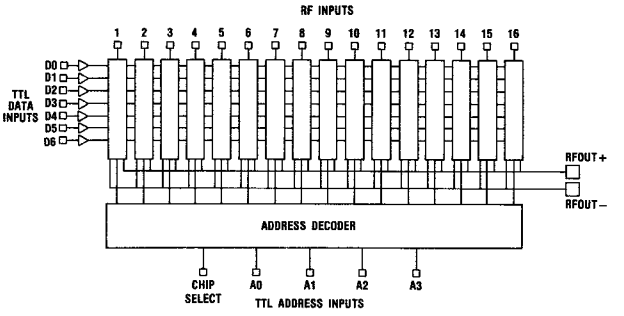

Figure 4. 16 Tap LSI GaAs IC Block Diagram.

CALIBRATION

Non-ideal gain states due to process variations contribute to tap weight implementation errors. The dual-gate FET transconductance standard deviation is about 10%. This translates into a RMS error over all tap weights of about 7% or 3 bits. Three bits of accuracy implies about 15dB sidelobes which is unacceptable. For this reason, a calibration procedure has been developed.

Each 7 bit unit cell has 128 gain states, Figure 5 is a plot of programmed gain versus measured gain for all 128 states of a unit cell. Calibration simply stores the tap weights for the measured gain closest to the ideal for each desired gain value For example, shown in Figure 5, the programmed gain must be 0.4 (00100 equivalent bit representation) to achieve an actual gain of 0.5. The calibration is calculated once and stored in a PROM. A 64 tap, 7 bit design would require 57Kbits to store the calibration, which is only one 8Kx8 PROM.

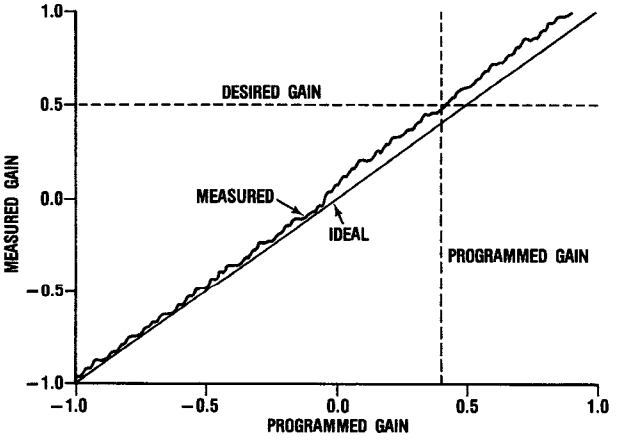

Figure 5. Actual Gain vs Programmed Gain for all 128 Gain States of a Typical DCVGA.

Multiple field GaAs slices were fabricated which contained the 16 tap array and several test structure. RF measurements on the unit cell, at 300MHz, show a calibrated accuracy of .9% RMS which is >6 bits equivalent accuracy, this implies 35 dB sidelobes for a 32 tap filter. Figure 6 shows the amplitude errors calibrated and uncalibrated at 300MHz. RMS errors rather than peak errors affect sidelobe performance. RF measurements also show little degradation in calibrated accuracy up to 1 GHz.

32 TAP FILTER

Figure 7 is a photograph of the experimental PTF. Two identical 16 tap LSI GaAs ICs (Figure 8) are wire bonded to a 32 tap $LiNbO_3$ SAW device. A 310 MHz center frequency, 100 MHz bandwidth interdigital transducer launches the acoustic wave. This transducer is excited by a balanced drive minimizing electromagnetic coupling to the output transducer. RF coupling is fruther minimized by adding a ground plane on the entire periphery of the SAW device.

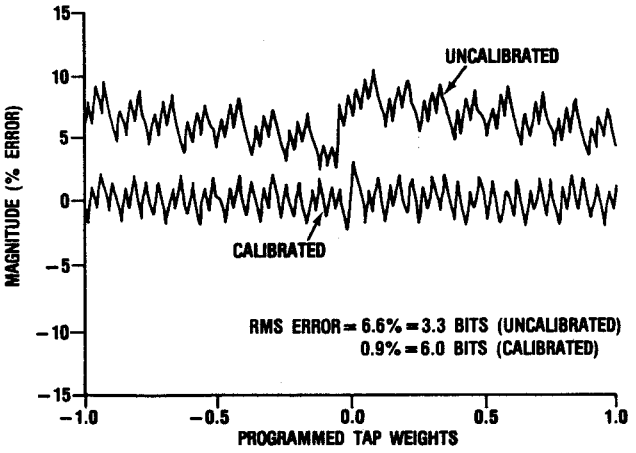

Figure 6. Measured DCVGA RF Gain Response Error (300 MHZ).

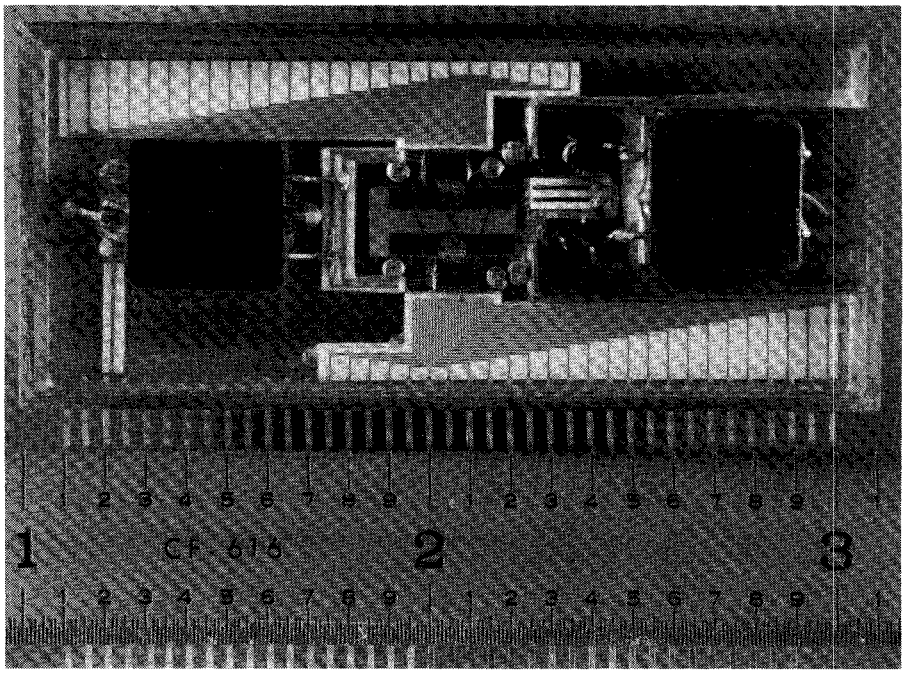

Figure 7. Photograph of Experimental SAW-PTF 32 Tap Filter.

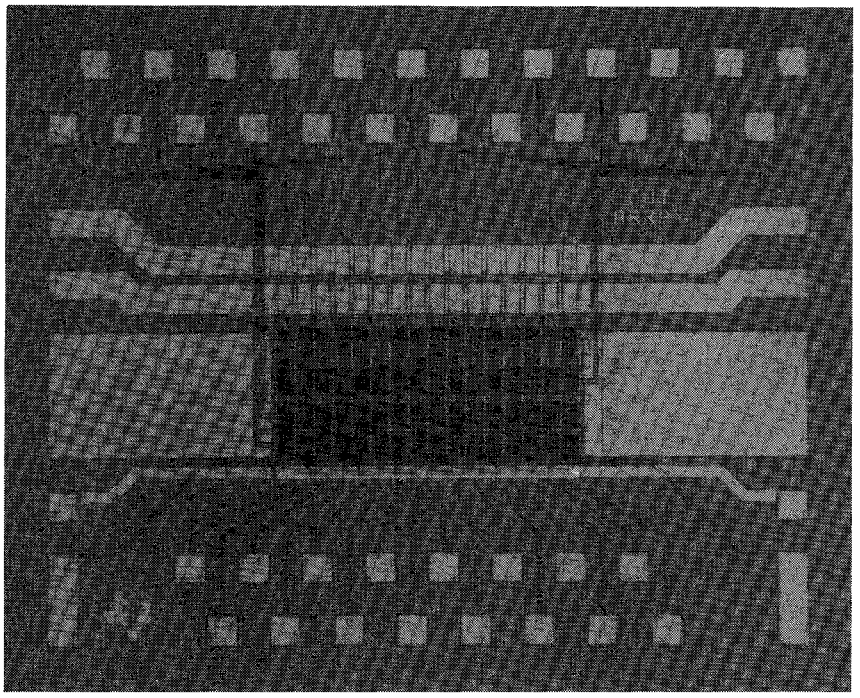

Figure 8. 16 Tap LSI GaAs IC.

The acoustic wave is detected by an array of 32 quarter wavelength (at 240MHz) active electrodes interleaved with ground electrodes. The active electrodes fanout to bond pads on both sides of the chip. The SAW device is fabricated using a three level process. The active electrodes are printed on the $LiNbO_3$, while the fanout to the bond pads is printed on polyimide to minimize parasitic capacitance.

CONCLUSION

The previous reported HPTF is limited in practicality by size. The DCPTF solves this problem with little sacrifice in performance. The DCPTF combines a $LiNbO_3$ SAW device for high dynamic range with digitally controlled GaAs ICs for precision tap weight control.

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